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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,446	10/29/2003	Arvind Kamath	03-1202/LSI1P233	7970

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EXAMINER	
SMOOT, STEPHEN W	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/697,446	KAMATH ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-15 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6 and 10* is/are allowed.

6)☒ Claim(s) *7,8,11-15 and 19-20* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 28 July 2005.

Claim Objections

1. Claim 11 is objected to because of the following informality:

In claim 11, line 6, change "the gate node" to --a gate node-- for proper antecedence.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7-8, 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "the grown dielectric oxide layer" in line 2; and

Claim 8 recites the limitation "the grown dielectric oxide layer" in line 2.

This limitation is indefinite because it does not particularly point out if it is supposed to be the first dielectric oxide layer from claim 1, lines 7-8 or the second dielectric oxide layer from claim 1, lines 8-9.

Regarding claim 20, the clause "an oxidizing ambient consisting of water" as used in claim 19, line 6 closes the claim to the inclusion of other ingredients in the oxidizing ambient besides water (see MPEP section 2111.03). However, claim 20, which depends on claim 19, attempts to limit the oxidizing ambient to also include "an ambient consisting of H and OH radicals" in line 2. Accordingly, claim 20 is vague because it does not distinctly claim the ingredients of the oxidizing ambient.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solo de Zaldivar (US 5,610,084) in view of Chau (US 5,763,922) and Chiao et al. (US 4,757,359).

Referring to Figs. 1a-1d, 3, 4a-4c and column 2, line 51 to column 5, line 43, Solo de Zaldivar disclose a method of forming an antifuse that includes the following features:

- A silicon substrate (1) with field oxide regions (6) is provided;
- A lower antifuse electrode (4) is formed in the silicon substrate (1) by n-type implanting through an oxide layer (14) corresponding to an exposed antifuse region as shown in Fig. 4a;
- A mask (22) is used to implant nitrogen (23) through the oxide layer (14) corresponding to the exposed antifuse region as shown in Fig. 4b;
- A 5 nm (i.e. 50 angstroms) thick antifuse oxide layer (3) and a 10 nm thick tunnel oxide layer (18) are then simultaneously grown by thermal oxidation as shown in Fig. 3;
- An upper antifuse electrode (5) is formed directly on the antifuse oxide (3); and
- The antifuse is programmed by applying a voltage of approximately 8 volts between the lower electrode (4) and the upper electrode (5) (see column 3, lines 5-20).

These are limitations set forth in claims 11, 15 of the applicant's invention.

However, Solo de Zaldivar does not expressly teach or suggest using wet oxidation with an ambient consisting of water for the thermal oxidation step, which is a limitation of claim 11. Also, Solo de Zaldivar lacks the step of determining the programmed state of the antifuse, which is also a limitation of claim 11. Further, Solo

de Zaldivar lacks the programming voltage being higher than the supply voltage feature of claim 15.

Chau teaches that an oxide layer can be grown on a silicon nitrogen layer by wet oxidation using a steam ambient (see column 8, lines 4-13). Chiao et al. teach that the programmed state of an oxide fuse can be read using a sense voltage of about 2 volts (see column 5, line 30 to column 6, line 2).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Solo de Zaldivar and Chau in order to grow the antifuse oxide layer of Solo de Zaldivar by wet oxidation using a steam ambient as taught by Chau. Chau recognizes that thermal oxidation by wet oxidation using a steam ambient results in the formation of a pure oxide layer that advantageously helps reduce hole injection from the overlying polysilicon gate electrode (see column 8, lines 4-13). It also would have been obvious to use a sense voltage as taught by Chiao et al. in order to determine if breakdown of the antifuse oxide layer of Solo de Zaldivar has occurred (i.e. to determine if the antifuse has been programmed).

6. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solo de Zaldivar (US 5,610,084), Chau (US 5,763,922), and Chiao et al. (US 4,757,359) as applied to claim 11 above, and further in view of Fifield et al. (US 2004/0004269 A1).

As shown above the combination of Solo de Zaldivar, Chau, and Chiao et al. has all of the limitations set forth in claim 11 of the applicant's invention. However, this combination lacks the switchably coupled feature of claim 12, the transistor connected

in series feature of claim 13, and the sense amplifier feature of claim 14. Referring to Fig. 6 and paragraphs [0039] to [0051], Fifield at al. teach an antifuse circuit that includes a current source (35) connected through a coupling transistor (36) to an antifuse element (200) and a transistor (31) for reading the antifuse (200) that is coupled to a voltage source (30) and a fuse latch (33). The read transistor (31) can operate as a switch or can be biased as an amplifier.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further combine the teachings of Solo de Zaldivar, Chau, and Chiao et al. with those of Fifield et al. in order to incorporate the antifuse circuit as taught by Fifield et al. Fifield et al. recognize that their antifuse circuit has the advantage of being able to read the programmed state of the antifuse independently from the actual antifuse programmed resistance (see paragraph [0051]).

7. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solo de Zaldivar (US 5,610,084) in view of Chau (US 5,763,922).

Referring to Figs. 1a-1d, 3, 4a-4c and column 2, line 51 to column 5, line 43, Solo de Zaldivar disclose a method of forming an antifuse that includes the following features:

- A silicon substrate (1) with field oxide regions (6) is provided;
- A lower antifuse electrode (4) is formed in the silicon substrate (1) by n-type implanting through an oxide layer (14) corresponding to an exposed antifuse region as shown in Fig. 4a;

- A mask (22) is used to implant nitrogen (23) through the oxide layer (14) corresponding to the exposed antifuse region as shown in Fig. 4b;
- A 5 nm (i.e. 50 angstroms) thick antifuse oxide layer (3) and a 10 nm thick tunnel oxide layer (18) are then simultaneously grown by thermal oxidation as shown in Fig. 3; and
- An upper antifuse electrode (5) is formed directly on the antifuse oxide (3).

These are limitations set forth in claim 19 of the applicant's invention.

However, Solo de Zaldivar does not expressly teach or suggest using wet oxidation with an ambient consisting of water for the thermal oxidation step, which is a limitation of claim 19. Also, Solo de Zaldivar lacks the use of shallow isolation trenches (also a limitation of claim 19) and, instead, teaches the use of field oxide regions (6) for defining active regions

Chau teaches that an oxide layer can be grown on a silicon nitrogen layer by wet oxidation using a steam ambient (see column 8, lines 4-13). Chau also teaches the use of shallow trench isolation regions (204 in Fig. 2) to electrically isolate an NMOS device (210) from a PMOS device (250) (see column 3, lines 12-13).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Solo de Zaldivar and Chau in order to grow the antifuse oxide layer of Solo de Zaldivar by wet oxidation using a steam ambient as taught by Chau. Chau recognizes that thermal oxidation by wet oxidation using a steam ambient results in the formation of a pure oxide layer that advantageously helps reduce hole injection from the overlying polysilicon gate electrode

(see column 8, lines 4-13). Also, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the teachings of Solo de Zaldivar by substituting shallow trench isolations, as taught by Chau, for the field oxide regions of Solo de Zaldivar because shallow trench isolations and field oxide regions are recognized in the art as equivalent ways to isolate active regions.

Regarding the H and OH radicals limitation of claim 20, this is a functional limitation that is presumed to be inherent to the above combination of Solo de Zaldivar and Chau because this combination is substantially identical to the applicant's as claimed process. Accordingly, per MPEP section 2112.01, a *prima facie* case of obviousness has been established and the burden shifts to the applicant to show that their method as claimed in claim 20 is different from the combination of Solo de Zaldivar and Chau.

Allowable Subject Matter

8. Claims 1-6, 10 are allowed.

9. Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of claim 19.

10. The following is a statement of reasons for the indication of allowable subject matter: Claims 1-6, 10 are allowed and claim 21 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a method of forming an antifuse on a semiconductor substrate that includes implanting nitrogen into a first portion of the substrate that corresponds to the antifuse combined with implanting nitrogen into a second portion of the substrate, wherein oxide layers are subsequently formed over both the first and second portions using the same wet oxidation step and the thickness of the oxide layers corresponding to the first and second portions are different.

Response to Arguments

11. Applicant's arguments with respect to claims 11-15 have been considered but are moot in view of the new grounds of rejection.

Conclusion

12. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

Stephen W. Smoot

STEPHEN W. SMOOT
PRIMARY EXAMINER